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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/845,455	04/30/2001	Kenneth James Kotlowski	P04920	3016
7590 10/03/2003				
Docket Clerk P O Drawer 800889 Dallas, TX 75380				
EXAMINER LEFKOWITZ, SUMATI				
ART UNIT		PAPER NUMBER		
2189				

DATE MAILED: 10/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/845,455

Applicant(s)

KOTLOWSKI ET AL.

Examiner

Sumati Lefkowitz

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 February 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 February 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-23 are pending.

Drawings

2. The drawings are objected to because

- in Figure 1, in block 130, "dispaly" should read --display--

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. The abstract of the disclosure is objected to because

- it contains the word "disclosed", more than 150 words in length, and is merely a recitation of one of the claims, not a concise statement of the technical disclosure of the patent, the statement including that which is new in the art to which the invention pertains, as is required by the guidelines for patent abstracts in the MPEP.

Correction is required. See MPEP § 608.01(b).

4. The disclosure is objected to because of the following informalities:

- on page 2, line 14 of the specification, the serial number of the related application is missing

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-3, 9-11, 17, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Ross et al., 5,909,594 (hereinafter Ross).

As to claims 1-3, 9-11, 17, and 18, Ross discloses a bus interface unit (note Figure 8, element 201, Figure 9, element 303) for transferring data between a plurality of bus devices (note Figure 8, devices 202-209, Figure 9, devices 301, 302), the bus interface unit comprising a first bus device interface (note Figure 9, link controller 304, wherein each link controller has a source link controller and a destination link controller as shown in Figure 10) comprising a first incoming request bus (note Figure 10, within link controller 304: port_req portion of switch 409 leading out of source link controller 401) for receiving request packets from a first one of the plurality of bus devices, a first outgoing request bus (note Figure 10, within link controller 304: port_req portion of switch 409 leading into destination link controller 402) for transmitting request packets to the first bus device, a first incoming data bus (note Figure 10, within link controller 304: bus leading through input packet buffer 406) for receiving data packets from the first bus device, a first outgoing data bus (note Figure 10, within link controller 304: bus leading to LLP send module 411) for transmitting data packets to the first bus device, a second bus

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device interface (note Figure 9, link controller 309) comprising a second incoming request bus (note Figure 10, within link controller 309: port_req portion of switch 409 leading out of source link controller 401) for receiving request packets from a second one of the plurality of bus devices, a second outgoing request bus (note Figure 10, within link controller 309: port_req portion of switch 409 leading into destination link controller 402) for transmitting request packets to the second bus device, a second incoming data bus (note Figure 10, within link controller 309: bus leading through input packet buffer 406) for receiving data packets from the second bus device, and a second outgoing data bus (note Figure 10, within link controller 309: bus leading to LLP send module 411) for transmitting data packets to the second bus device, and an arbitration circuit (note Figure 10, elements 410, 407) capable of determining a first priority level associated with a first request packet received from the first bus device and capable of determining a second priority level associated with a second request packet received from the second bus device, wherein the arbitration circuit compares the first priority level with the second priority level to determine which of the first and second priority levels is higher, wherein the arbitration circuit, in response to a determination that the first priority level is higher than the second priority level, causes the bus interface unit to process the first request packet prior to processing the second request packet (note column 14, line 41 – column 16, line 56), further discloses an integrated data circuit comprising N bus devices (note Figure 8, devices 202-209, Figure 9, devices 301, 302) capable of transferring data with one another, a bus interface unit (note Figure 8, element 201, Figure 9, element 303) for transferring data between the N bus devices, the bus interface unit comprising N bus interfaces (note Figure 9, link controllers 304, 309, i.e., one for each device coupled to the bus interface unit 303), each of the N bus interfaces

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comprising an incoming request bus (note Figure 10, port_req portion of switch 409 leading out of source link controller 401) for receiving request packets from one of the N bus devices, an outgoing request bus (note Figure 10, port_req portion of switch 409 leading into destination link controller 402) for transmitting request packets to the one of the N bus devices, an incoming data bus (note Figure 10, bus leading through input packet buffer 406) for receiving data packets from the one of the N bus devices, and an outgoing data bus (note Figure 10, bus leading to LLP send module 411) for transmitting data packets to the one of the N bus devices, and an arbitration circuit (note Figure 10, elements 410, 407) capable of determining a first priority level associated with a first request packet received from a first bus device and capable of determining a second priority level associated with a second request packet received from a second bus device (note column 14, line 41 – column 16, line 56).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

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invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 4, 12, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ross et al., 5,909,594 (hereinafter Ross) in view of Simpson et al., 6,185,629 (hereinafter Simpson).

As to claims 4, 12, and 19, Ross fails to disclose that the arbitration circuit, in response to a determination that the first priority level is equal to the second priority level, causes the bus interface unit to process the first and second request packets on a rotating turn basis.

Simpson discloses that an arbitration circuit, in response to a determination that a first priority level is equal to a second priority level, grants the first and second request packets on a rotating turn basis (note column 23, lines 34-43 and column 25, lines 17-27).

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the use of a rotating arbitration scheme if requests are of equal priority, as Simpson teaches, in the system of Ross, so as to insure that no request packets are starved of service, thereby promoting a fair arbitration scheme.

9. Claims 5-8, 13-16, and 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ross et al., 5,909,594 (hereinafter Ross) in view of Azevedo et al., 4,969,120 (hereinafter Azevedo).

As to claims 5-8, 13-16, and 20-23, Ross fails to disclose the arbitration circuit comprising a time slice timer capable of producing a current time slice value, wherein the arbitration circuit is capable of determining a fixed time slice range associated with the first bus

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device and comparing the fixed time slice range with the current time slice value, wherein the arbitration circuit, in response to a determination that the current time slice value is within the fixed time slice range, causes the bus interface unit to process the first request packet prior to processing the second request packet or wherein the arbitration circuit, in response to a determination that the current time slice is within the fixed time slice range, causes the bus interface unit to process the first request packet prior to processing any pending request packet received by the bus interface unit.

Azevedo discloses an arbitration circuit comprising a time slice timer (i.e., counter 25) capable of producing a current time slice value, wherein the arbitration circuit is capable of determining a fixed time slice range associated with a first bus device and comparing the fixed time slice range with the current time slice value, wherein the arbitration circuit, in response to a determination that the current time slice value is within the fixed time slice range, causes servicing of a first request prior to servicing of a second request, wherein the arbitration circuit, in response to a determination that the current time slice is within the fixed time slice range, causes servicing of the first request prior to servicing any pending request received (note column 2, lines 3-20 and column 3, line 16 – column 4, line 40).

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the use of time slotted arbitration, as Azevedo teaches, in the system of Ross so as to insure that certain high priority devices are fairly guaranteed resource access over non-high priority devices.

Conclusion

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10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, as the prior art teaches or suggests bus interfaces comprising unidirectional, point-to-point links/paths.

US PG-PUBS:	2002/0126693 Stark et al.	2002/0120878 Lapidus
	2002/0118041 Lapidus	2002/0110120 Hagglund et al.
	2002/0053004 Pong	
US Patents:	6,584,101 Hagglund et al.	6,581,116 Arimilli et al.
	6,504,817 Oldfield et al.	6,415,424 Arimilli et al.
	6,353,867 Qureshi et al.	6,282,195 Miller et al.
	6,256,693 Platko	6,205,524 Ng
	6,145,039 Ajanovic et al.	5,991,824 Strand et al.
	5,859,550 Brandt	5,634,043 Self et al.
	5,623,644 Self et al.	5,581,729 Nishtala et al.
	5,539,739 Dike et al.	

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sumati Lefkowitz whose telephone number is 703-308-7790.

The examiner can normally be reached on Monday-Friday from 6:00-2:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached at 703-305-4815.

The fax phone numbers for the organization where this application or proceeding is assigned are:


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703-746-7238 for After-Final communications

703-872-9306 for Official communications

703-746-5661 for Non-Official/Draft communications

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.



Sumati Lefkowitz
Primary Examiner
Art Unit 2189

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September 25, 2003